Commissioner for Patents

REMARKS

The above-noted amendments are presented in response to the Office Action of February 10, 2003, wherefore reconsideration is requested.

Referring now to the text of the Office Action:

a) claims 1-5 and 67-68 stand rejected under 35 U.S.C. § 102(b), as being unpatentable over the teaching of United States Patent No. 5,757,857 (Buchwald);

b) claims 32-35 stand rejected under 35 U.S.C. § 102(b), as being unpatentable over the teaching of United States Patent No. 5,889,828 (Miyashita et al.) and

c) claims 6-31, 36-66 and 69-78 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

As an initial matter, applicant appreciates the Examiner's indication of allowable subject matter in claims 6-31, 36-66 and 69-78. It is believed that the Examiner's objections to the rejected claims 1-5, 32-35 and 67-68 are overcome by the above-noted claim amendments, and further in view of the comments below.

United States Patent No. 5,757,857 (Buchwald) teaches a clock recovery circuit for recovering a clock signal from an NRZ data signal. As shown in FIGs. 8 and 10, the NRZ data (at 34) is filtered to produce a filtered data signal (at 36). The filtered data signal is sampled by first and second sample and hold circuits 48 and 50. These sample and hold circuits operate at a timing of a clock signal generated by VCO 60, and produce respective output signals that indicate the level of the filtered data signal at the timing of

Commissioner for Patents

the clock signal. The first sample and hold 48 is triggered by an in-phase clock signal (rising edges of the VCO signal), and thus samples upper and lower peak valves of the filtered data signal. The output of the first sample and hold circuit is digitized by a limiter circuit 52 which "cleans up the noise from sample and hold 48 and outputs an unambiguous high and low logic signals" (Col 9, lines19-21). This digitized signal is output from the clock recovery circuit as the recovered data signal. The second sample and hold 50 is triggered by a quadrature clock signal (actually falling edges of the VCO signal), and thus samples transitions of the filtered data signal. The output of the second sample and hold 50 comprises "cross-over samples" which contain the phase error information as illustrated in FIGs. 9a-c (Col 9, lines 25-29). Thus it will be seen that the first and second sample and hold circuits sample the filtered DATA signal at a timing of the VCO clock.

The third sample and hold 56 samples the cross-over samples generated by the second sample at a timing of rising edges of the recovered data signal generated by limiter 52, in order to extract the phase error information.

Referring to Col 3, lines 54-58, Buchwald states that "for the purpose of this specification a sample and hold circuit shall be defined to include any circuit which performs an equivalent function to a sample and hold circuit, such as a tracking and hold circuit." In the embodiments of FIGs. 3 and 4, each sample and hold circuit 48, 50 and 56 is provided by a respective pair of parallel track-and-hold circuits 64-66; 68-70 and 78-8, cascaded with a multiplexer 72, 74, and 84. As is well known in the art, such circuits operate to generate a DC output voltage level substantially equal to the input signal voltage at the timing of the rising or falling edge of a latch signal (in this case, the VCO 60 clock). This is inherently an analog function, since the output voltage can be any value taken by the input signal. Thus it will be seen that the sample and hold circuits of Buchwald must necessarily be analog circuits.

Commissioner for Patents

In direct contrast, the present invention teaches first and second digital sample means which sample the clock signal, at a timing of the data signal, to generate respective beat signals. This functionality is neither taught nor suggested by Buchwald. As described in the present application, the digital sample means of the present invention are preferably provided by flip-flop circuits. As is well known, flip-flop circuits output a digital signal that corresponds to the logic state (rather than the voltage level per se) of the input signal. As such, the skilled artisan will recognize that the digital sample means of the present invention are in no way equivalent to the sample and hold circuits of Buchwald. Furthermore, in accordance with the present invention, the digital sample means operate to sample the clock signal at a timing of the data signal. This is in no way equivalent to the arrangement of the Buchwald patent, in which the (filtered) data is sampled at a timing of the VCO clock. Accordingly, it is submitted that the present invention is clearly distinguishable over the teaching of Buchwald.

With respect to the Examiner's rejection of claims 32-35 in light of United States Patent No. 5,889,828 (Miyashita et al.), applicant notes that Miyashita et al do not teach or suggest the features of the digital frequency detector as defined in amended claim 32. Thus it is believed that independent claim 32 (as now amended) is clearly distinguishable over the teaching of Miyashita et al.

In light of the foregoing, it is believed that the present application is in condition for allowance, and early action in that respect is courteously solicited.

If any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this response, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees

Commissioner for Patents

required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 19-5113.

Reconsideration of this application is requested.

Respectfully submitted,
James MOSER

By _____
Kent Daniels
Registration No. 44,206
Attorney for Applicant

KD/nt
Date: August 11, 2003

Ogilvy Renault
Suite 1600
1981 McGill College Anvenue
Montreal, Quebec
Canada, H3A 2Y3

(613) 780-8673